REMARKS

The Examiner's Office Action of December 13, 2002 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

By the above actions, claim 1 has been amended and new claims 12 and 13 been added. Claims 8-11 have been withdrawn from consideration in the Response filed November 18, 2002. Accordingly, claims 1-7, and 12-13 are pending for consideration, of which claim 1 is independent. In view of these actions and the following remarks, reconsideration of this application is now requested.

Referring now to the detailed Office Action, the specification is objected to as the title of the invention is not descriptive. In response, Applicants have amended the title, as shown above.

Claims 1-7 stand rejected under 35 U.S.C. §103(a) as unpatentable over Kitch (U.S. Patent No. 6,200,90) in view of Edelstein et al. (U.S. Patent No. 6,181,02 – hereafter Edelstein). This rejection is respectfully traversed at least for the reasons provided below.

In order to overcome the problem of forming a void in a plug formed in a via hole when the via hole has a high aspect ratio, the present invention in accordance with amended claim 1 comprises metal interconnects made from a multi-layer film composed of a first metal film deposited on a semiconductor substrate with an insulating film sandwiched therebetween and a second metal film deposited on the first metal film; an interlayer insulating film formed over the metal interconnects; and a plug made from a third metal film provided within a via hole formed in the interlayer insulating film, wherein the third metal film is selectively grown on the second metal film contacted with a bottom of said via hole. In order to facilitate the comparison of the presently claimed invention and that of the prior art references, Applicants are describing the present invention herein using numerically labeled features as examples.

Turning to Kitch, Kitch teaches that in a multi-layer interconnect structure (20) having air voids (29), a metal nitride layer (CuN) (26), serving as an etch stop, is formed between a plug (Cu) (27) and an interconnect (Cu) (25). According to Kitch, the multi-layer interconnect structure (20) has not only a dielectric layer (30) having air voids (29), but also an additional

dielectric material (32) formed, by filling up using CMP, on the metal interconnect (25) and besides the layer of conductive metal (27). In other words, the interlayer insulating film in Kitch is composed of both the dielectric layer (30) and the additional dielectric material (32).

However, according to the present invention, the interlayer insulating film (116) is formed over the metal interconnects (114). In other words, the interlayer insulating film (116) in the present invention is composed of only insulating film, which is different from Kitch.

With respect to Edelstein, Edelstein teaches forming an alloy seed layer (86) on a conductivity diffusion barrier layer (72) to improve the adhesion between a copper plug (60) and the barrier layer (72). According to Edelstein, the seed layer (86) is formed on the barrier layer (72), which is formed within the entire inner portion of an opening (84). In other words, the copper plug (60) is formed not only on the bottom, but also on the sides of the opening (84). Moreover, in order to improve the adhesion between the copper plug and the barrier layer, it is required of the seed layer to be formed on the barrier layer.

However, according to amended claim 1 of the present invention, the second metal film (105), which is a seed layer, is formed as an upper layer of the metal interconnects (114) below the via hole (109). Hence, the plug (112), i.e., third metal film, is selectively grown on the second metal film contacted with the bottom of the via hole (109). Moreover, unlike Edelstein which require the seed layer to be formed on the barrier layer, there is no seed layer on a barrier layer is included in the presently claimed invention.

According to Kitch, the barrier layer is formed covering the multi-layer interconnect structure (20) during the forming of the plug (27) and the interconnect (25) using copper (column 3, lines 31-36). In other words, no barrier layer is formed between the plug (27) and the interconnect (25). Hence, there is no motivation in combining Kitch and Edelstein, in which the seed layer is formed on the barrier layer.

Further, even if Kitch is combined with Edelstein, since the seed layer is formed within the entire inner portion of an opening, the combination fails to disclose the features and effects of the present invention.

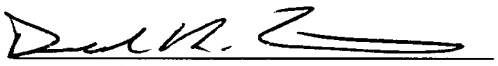
The requirements for establish a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or

motivation, either in the reference themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. As Kitch and Edelstein are deficient, as discussed above, and there is no reasonable expectation of success in combining their different teachings to arrive at the presently claimed invention, their combination in a §103(a) rejection would be improper.

In view of the amendments and arguments set forth above, Applicants respectfully request reconsideration and withdrawal of all the pending rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,



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MARKED UP VERSION

1. (Amended) A semiconductor device comprising:

metal interconnects made from a multi-layer film composed of a first metal film deposited on a semiconductor substrate with an insulating film sandwiched therebetween and a second metal film deposited on said first metal film[;] wherein the second metal film is a seed layer;

an interlayer insulating film formed [on] over said metal interconnects; and

a plug made from a third metal film [selectively grown on said second metal film] provided within a via hole formed in said interlayer insulating film,

wherein said third metal film is selectively grown on said second metal film contacted with a bottom of said via hole.